James Mackenzie, EIT

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PROFILE

James Mackenzie is a computer engineer with experience in software development and ASIC design and verification. He has consistently exceeded past employers' needs and expectations with his ability to quickly and efficiently learn and deploy new languages and skill sets.

Through four co-op work terms and full-time work at Intel, James has proven his ability to rapidly troubleshoot, diagnose, and resolve complex technical issues in a variety of areas. His current role at Intel allows him to design, develop, and verify the next generation of Intel datacenter SSDs, while his two work terms at Intel prior to graduation focused mainly on block-level verification. Prior to those roles, James worked at IBM in a software engineering role, where he was a member of a multinational team developing a high-value consumer-facing software product. He has also worked at Wind River, where he designed and developed a number of internal tools for Wind River Education Services.

SKILLS

Languages:	SystemVerilog, Python, Java, SystemRDL.
Software:	Synopsys VCS/Design Compiler/Spyglass, Denali Blueprint, DVCSs.
Hardware:	NVMe, PCI/PCIe, AXI3/4/4-Lite.

WORK EXPERIENCE

SoC Design Engineer, Intel; Vancouver, BC, Canada
January 2016-Present

- Applied experience gained in software and hardware design to the verification of ASIC RTL designs using SystemVerilog and UVM.
- Verified RTL designs from a blank-slate UVC and test plan to 100% coverage closure.
- Developed and maintained RTL designs from initial planning to post-tapeout.
- Successfully prepared RTL designs for delivery using Spyglass and Design Compiler.
- Acted as supervisor to co-op students and successfully ramped them into productive members of the ASIC design and verification team.
- Developed methodologies and internal IP to improve the verification team’s productivity and effectiveness.
- Gained significant in-depth experience in SSD architecture, specifically in NVMe over PCIe.

Component Design Engineer (Co-op), Intel; Vancouver, BC, Canada
May 2014-August 2014 and May 2013-December 2013

- Verified block-level designs of ASICs using SystemVerilog and constrained random testing.
- Designed and maintained UVM-based testbenches using cutting-edge standards.
- Created and enhanced stimulus generators, monitors, and scoreboards.
- Developed testing and coverage plans and drove functional coverage to completion.
- Created and maintained Python scripts to aid in verification tasks.

Software Development Engineer (Co-op), IBM; Victoria, BC, Canada
September 2012-December 2012

- Fixed defects in and added new features to a major consumer-facing Java-based IBM product.
- Participated as a member of an international team in a challenging and rewarding environment.
- Created automated JUnit test suites in preparation for a major product release.
- Aided in rewriting a program installer with the end goal of compatibility with Windows 8.

Software Development Engineer (Co-op), Wind River Systems; Ottawa, ON, Canada
January 2012-April 2012

- Developed a number of subsystems for an internal automated GUI testing system using Python and Qt.
- Led the design and development of an internal file sharing website using Python, PHP, HTML, and CSS. The system was successfully deployed on multiple servers around the world and was capable of automatically ensuring file redundancy and availability.
- Engineered an online dashboard in PHP that allowed engineers to see how customers rated their work.

EDUCATION

B.Eng, Computer Engineering, University of Victoria. Specialization in Embedded Systems.

PROJECTS AND CLUBS

Little Dog; University of Victoria — 2015

The major term project of CENG 441 (Design of VLSI Systems), with team members from CENG 499 (Design Project II) and MECH 400 (Design Project). Led development and testing of a number of internal blocks for an FPGA-based PD control system for a quadruped rover using VHDL. The control system was designed such that all 12 motors of the rover were able to process and drive positional updates independently of each other. Also led integration and verification efforts of the overall design using ModelSim. Awarded the Design Technical Project Award (first place) by the IEEE Victoria Chapter out of 30 teams.

Third Eye; University of Victoria — 2015

The major term project of CENG 490 (Design Project II). Led development and hardware engineering of a blind spot traffic detection system for cyclists. Made use of ultrasonic sensors, an Arduino, and BLE to communicate traffic data to an iPhone. The iPhone app allowed users to listen to their own music while traveling, as the app would lower the volume of the music or play an alert if a threat was closing on them depending on the threat's closing speed and distance. Awarded the Design Technical Project Award (second place) by the IEEE Victoria Chapter out of 15 teams.

Pipelined Processor; University of Victoria — 2015

The major term project of CENG 450 (Processor Design). Given a RISC-like instruction set, worked in a team of two to design and implement a pipelined processor on an FPGA using VHDL. The design utilized multi-port memories and had the ability to process instructions that spanned multiple PC counts in a single clock cycle.

Tiny Space Battles; University of Victoria — 2014

The major term project of CENG 356 (Engineering System Software). Sole developer and designer of a networked multiplayer video game implemented in Python. Using a Nintendo Wii Remote connected via Bluetooth or the keyboard, two players fought to destroy each other's spaceship.

Student Mentor; University of Victoria — 2014

Acted as a mentor to two first-year engineering students as a part of a select course that focused on instilling the values of professional practice to engineering students. Helped guide students into education paths that they found enjoyable and enlightening while ensuring they were afforded all reasonable help possible to get through first year.

AWARDS

Design Technical Project Award (First Place); University of Victoria — 2015
Awarded to the first place winner of the IEEE Victoria Design Competition for the Little Dog project out of 30 teams. All graduating University of Victoria engineering students take part in the competition as part of their final design project. The projects are judged by a panel of practicing IEEE Victoria Chapter members and University of Victoria faculty members.

Design Technical Project Award (Second Place); University of Victoria — 2015
Awarded to the second place winner of the IEEE Victoria Design Competition for the Third Eye project out of 15 teams. All graduating University of Victoria engineering students take part in the competition as part of their final design project. The projects are judged by a panel of practicing IEEE Victoria Chapter members and University of Victoria faculty members.

ACTIVITIES AND INTERESTS

Running, bicycling, photography, hiking, English literature, quantum physics, public speaking, mentorship, leadership.